2PARMA Project

PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures

HiPEAC Clusters Meeting, Chamonix, April 7th, 2011

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FP7-248716-2PARMA Project

List of Project Partners

1. Politecnico di Milano (POLIMI) – Italy **(Coordinator)**
2. STMicroelectronics (STM) – Italy
3. Fraunhofer Institut for Telecommunications / Heinrich-Hertz Institut (HHI) – Germany
4. Interuniversitair Micro-Electronica Centrum (IMEC) – Belgium
5. Institute of Communication and Comp Systems (ICCS) - Greece
6. RHEINISCH-WESTFAELISCHE TECHN HOCHSCHULE AACHEN (RWTH) - Ger
7. Synopsys (CoWare) - Belgium

Project Coordinator
prof. Cristina SILVANO, POLIMI
Project Technical Manager
prof. William Fornaciari, POLIMI
Start date: January 1st, 2010
Project duration: 3 years
Total effort: 408 PM
EC Contribution: 2.74 M€
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April 7th, 2011

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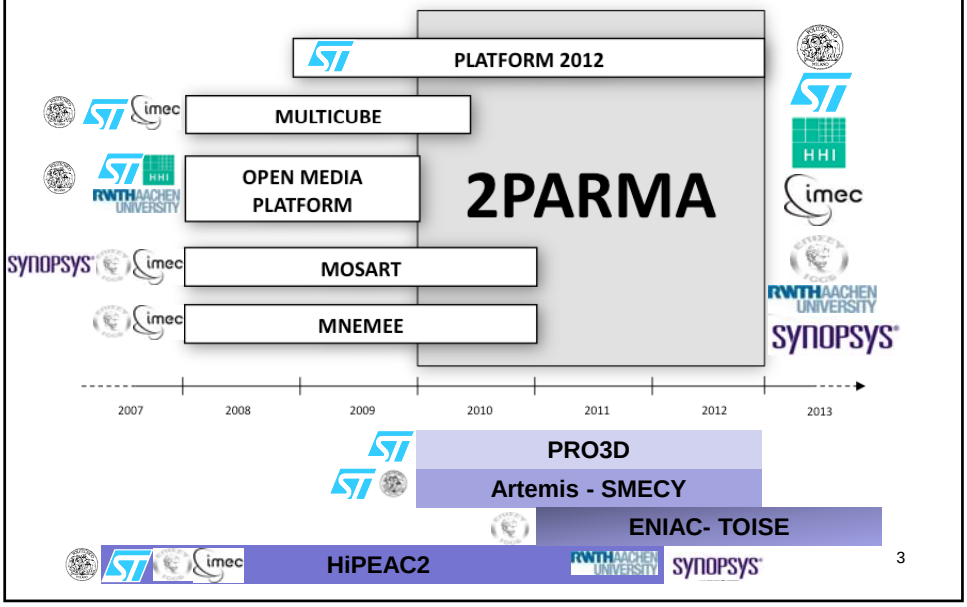
Back-ground & side-ground projects



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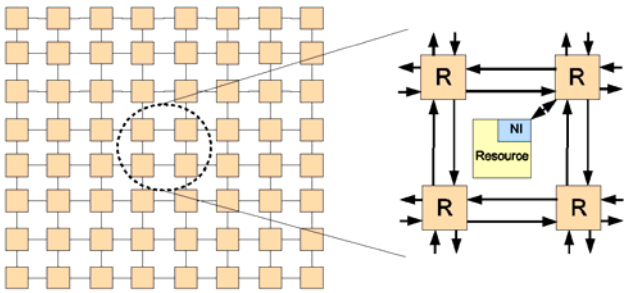
Scientific and Technical Objectives

Main Goals	Project Outcomes
• Programmability of Many-core Computing Fabrics • Virtualisation and Continuous Adaptation	• Integrated Compiler Toolchain and OS Layer
• Design Space Exploration	• DSE Toolchain
• Runtime Adaptivity	• Run-time Resource Manager

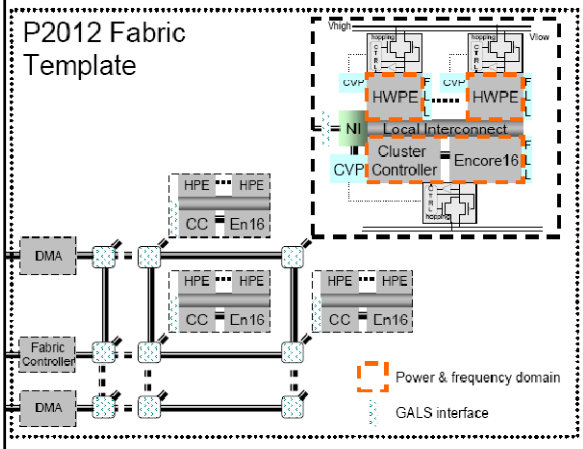
The 2PARMA project focuses on the definition of suitable parallel programming models, instruction set virtualisation, run-time energy/power and resource management policies and mechanisms as well as design space exploration methodologies for Many-core Computing Fabrics.

Many-Core Computing Fabric Template



*The 2PARMA project focuses on the flexible family of parallel and scalable computing processors, which we call **Many-core Computing Fabric Template,** composed of many processing cores interconnected by an on-chip network.*

Platform 2012: Scalable Architecture Template

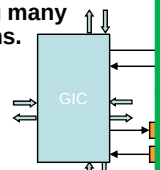


Platform 2012: A Many-core Programmable Accelerator for Ultra-Efficient Embedded Computing in Nanometer Technology

Source: STMicroelectronics

P2012 Cluster

- **Cluster Architecture evolutions supporting many applications.**



- **Heterogeneous Cluster RTL implementation(s):**
  - ENCore<N>,
  - Cluster Controller,
    - Cluster Control,
    - DMA Control,
  - Debug logic,
  - Stream-flow logic,
  - User-def. HWPEs.

User-defined HWPEs

Stream-flow logic

Inter-HWPE communication,
L3 or shared Memory ⇔ HWPEs communication.

Cluster Control

ENCore Boot, HWPE control, etc…

DMA Control

L3 ⇔ Sh. Mem., L3 ⇔ Stream, Sh. Mem. ⇔ Stream

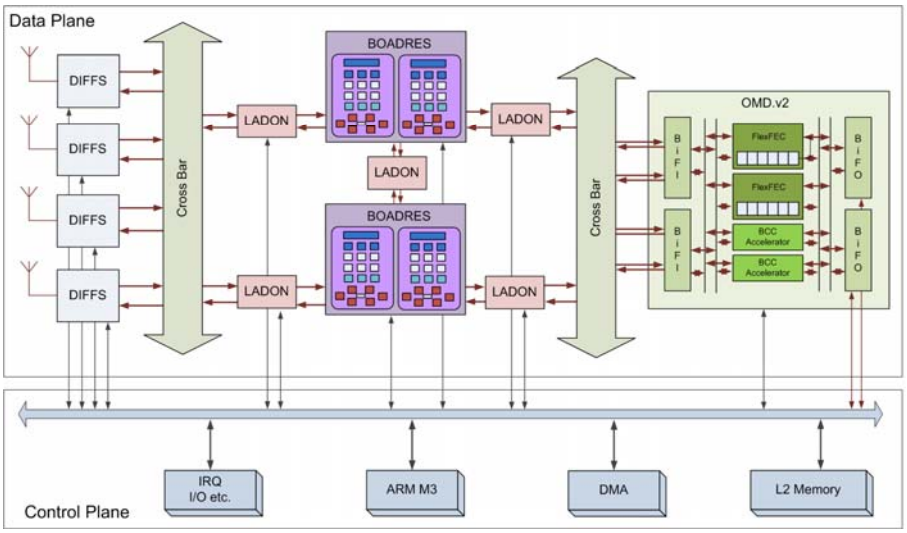
Configurable
(N, EFUs, banking factor, …)
"Computing Farm"
(supplied by "Computing")

For SW PEs and/or intensive control

Debug *Multicore Debug*

Source: STMicroelectronics

IMEC COBRA Platform



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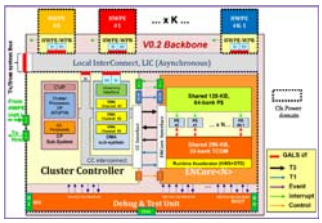
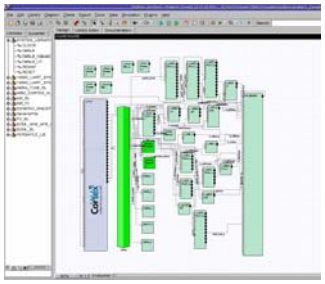
Synopsys Virtual Platforms

1. Abstract model mimicking P2012 in support of CBSE methodology

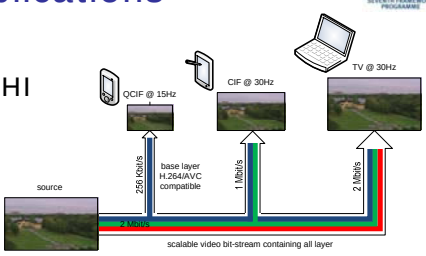


2. ARM based multi-core platform supporting Linux OS for design tool validation
   - Integration with DSE tools
   - Investigate RTRM support

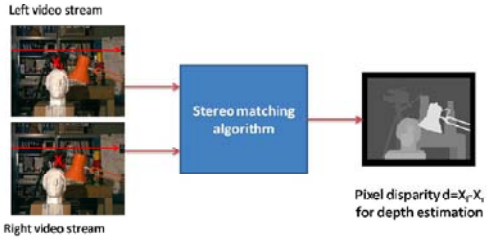


2PARMA Target Applications

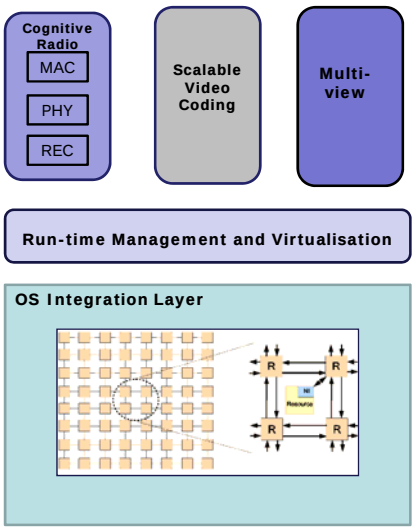
- Scalable Video Coding (SVC) – HHI



- Cognitive Radio
  - Physical Layer – RWTH-ISS
  - MAC Layer – RWTH-iNETs
  - Reconfigurable Radio – IMEC
- Multi-view Image Processing - IMEC

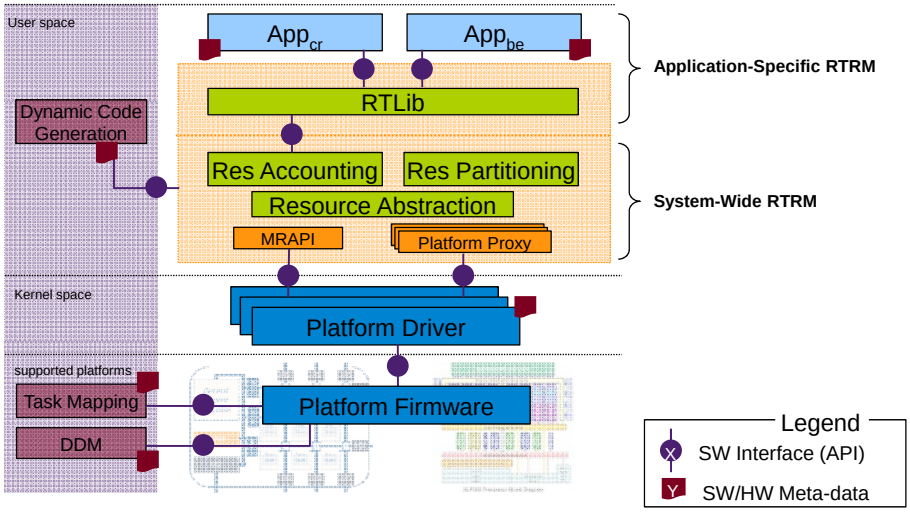


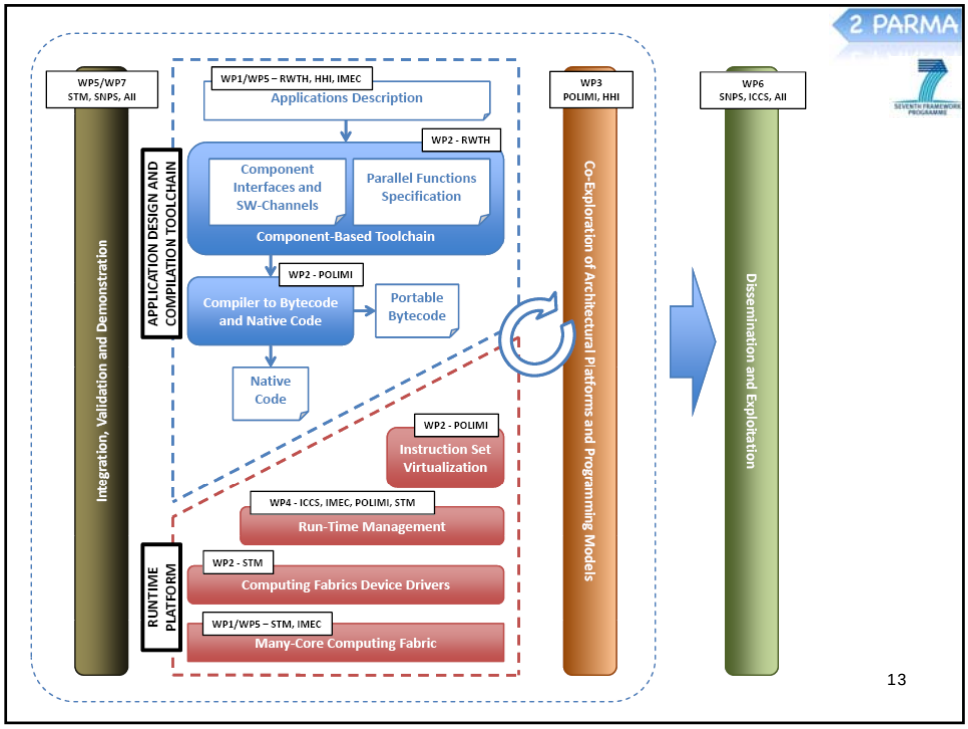
Applications/Architecture Integration



The 2PARMA Run-Time Resource Manager

Overall view




2 PARMA
WP5/WP7
STM, SNPS, All
WP1/WP5 – RWTH, HHI, IMEC
Applications Description
WP2 - RWTH
Component Interfaces and SW-Channels
Parallel Functions Specification
Component-Based Toolchain
APPLICATION DESIGN AND COMPILATION TOOLCHAIN
WP2 - POLIMI
Compiler to Bytecode and Native Code
Portable Bytecode
Native Code
WP3
POLIMI, HHI
Co-Exploration of Architectural Platforms and Programming Models
WP6
SNPS, ICCS, All
Dissemination and Exploitation
Integration, Validation and Demonstration
WP2 - POLIMI
Instruction Set Virtualization
WP4 - ICCS, IMEC, POLIMI, STM
Run-Time Management
RUNTIME PLATFORM
WP2 - STM
Computing Fabrics Device Drivers
WP1/WP5 – STM, IMEC
Many-Core Computing Fabric
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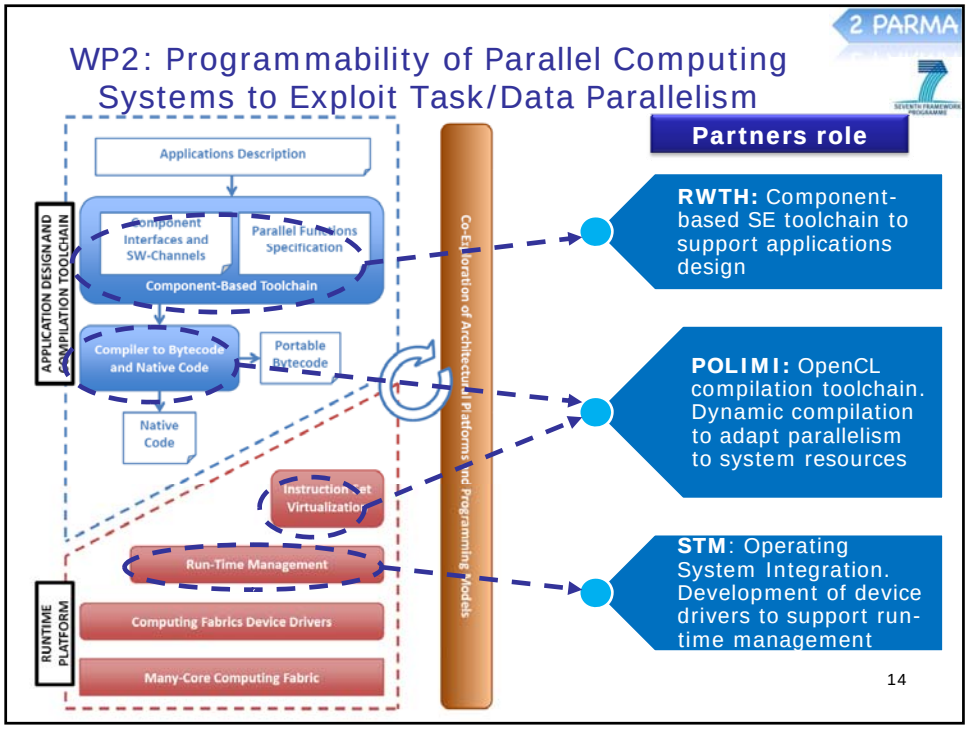
2 PARMA
WP2: Programmability of Parallel Computing Systems to Exploit Task/Data Parallelism
Partners role
Applications Description
Component Interfaces and SW-Channels
Parallel Functions Specification
Component-Based Toolchain
APPLICATION DESIGN AND COMPILATION TOOLCHAIN
Compiler to Bytecode and Native Code
Portable Bytecode
Native Code
Instruction Set Virtualization
Run-Time Management
Computing Fabrics Device Drivers
Many-Core Computing Fabric
RUNTIME PLATFORM
Co-Exploration of Architectural Platforms and Programming Models
RWTH: Component-based SE toolchain to support applications design
POLIMI: OpenCL compilation toolchain. Dynamic compilation to adapt parallelism to system resources
STM: Operating System Integration. Development of device drivers to support run-time management
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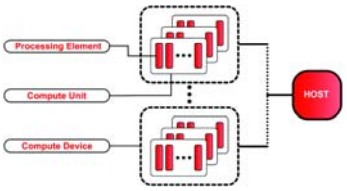
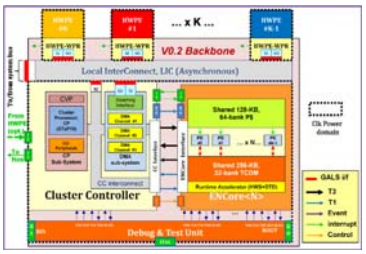
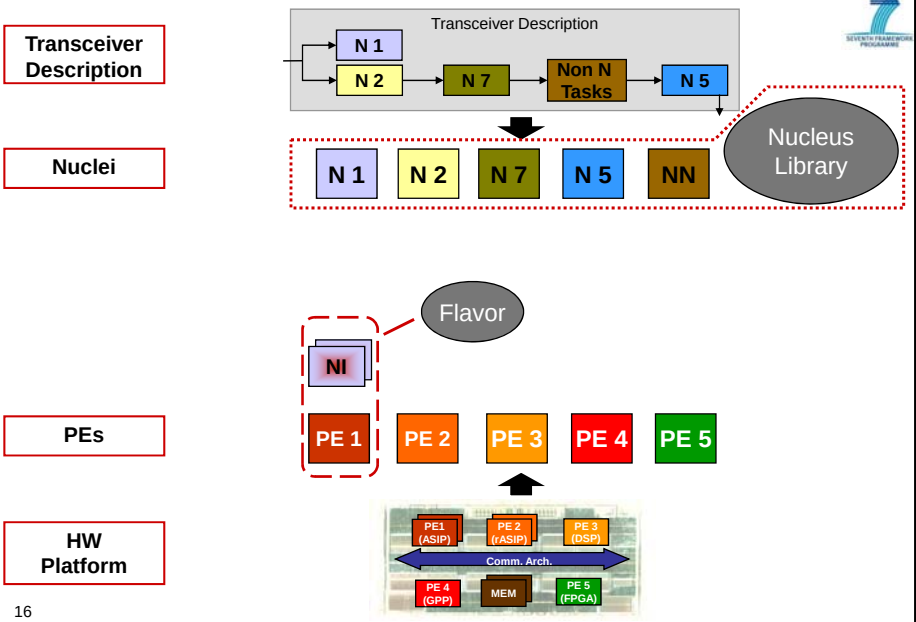
Mapping OpenCL to Computing Fabrics

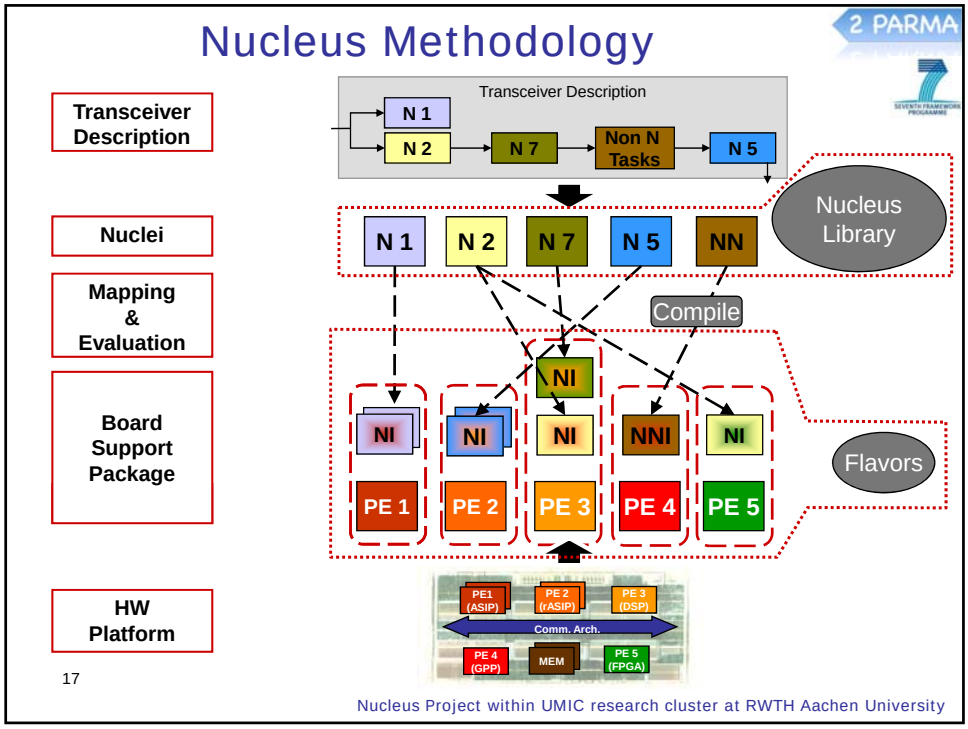
- Analysis of OpenCL programming model (strengths and weaknesses) vs P2012 Computing Fabric
- Specification of Computing Fabric-specific extensions to OpenCL
- Proposed OpenCL extensions targeting Computing Fabrics
- OpenCL front-end compilation toolchain for LLVM to be publicly released soon
- Dynamic compilation to adapt parallelism to system resources





Nucleus Methodology




Nucleus Methodology
2 PARMA
Transceiver Description
Nuclei
Mapping & Evaluation
Board Support Package
HW Platform
Transceiver Description
N 1
N 2
N 7
Non N Tasks
N 5
Nucleus Library
N 1
N 2
N 7
N 5
NN
Compile
NI
NNI
Flavors
PE 1
PE 2
PE 3
PE 4
PE 5
PE1 (ASIP)
PE 2 (rASIP)
PE 3 (DSP)
Comm. Arch.
PE 4 (GPP)
MEM
PE 5 (FPGA)
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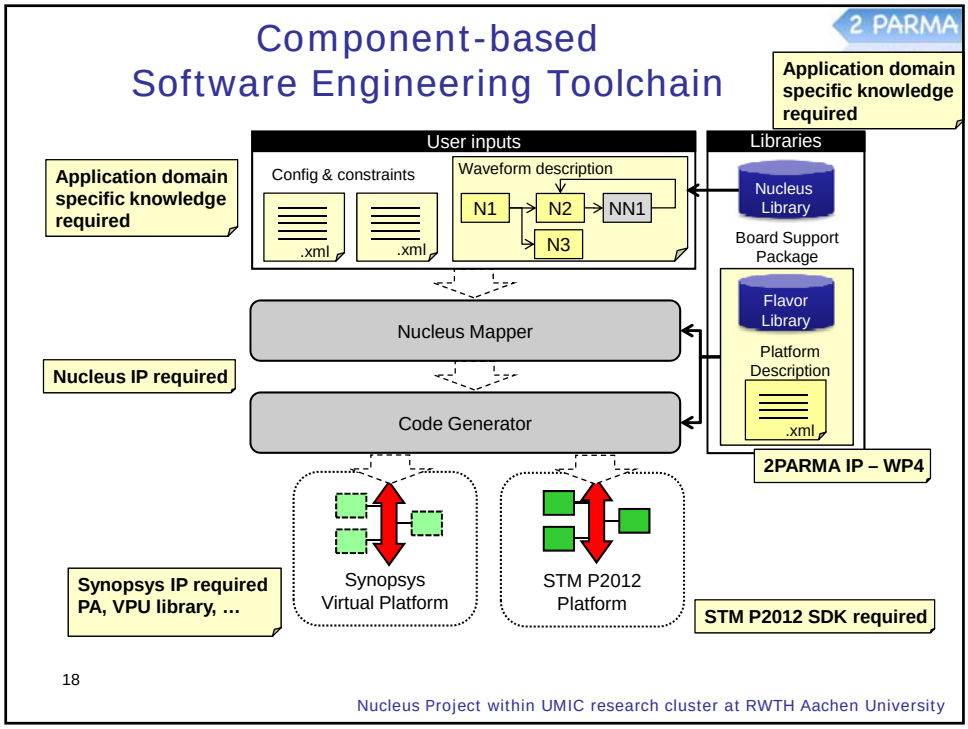
Nucleus Project within UMIC research cluster at RWTH Aachen University


Component-based Software Engineering Toolchain
2 PARMA
Application domain specific knowledge required
User inputs
Libraries
Application domain specific knowledge required
Config & constraints
.xml
.xml
Waveform description
N1
N2
NN1
N3
Nucleus Library
Board Support Package
Flavor Library
Platform Description
.xml
Nucleus Mapper
Nucleus IP required
Code Generator
2PARMA IP – WP4
Synopsys Virtual Platform
STM P2012 Platform
Synopsys IP required PA, VPU library, …
STM P2012 SDK required
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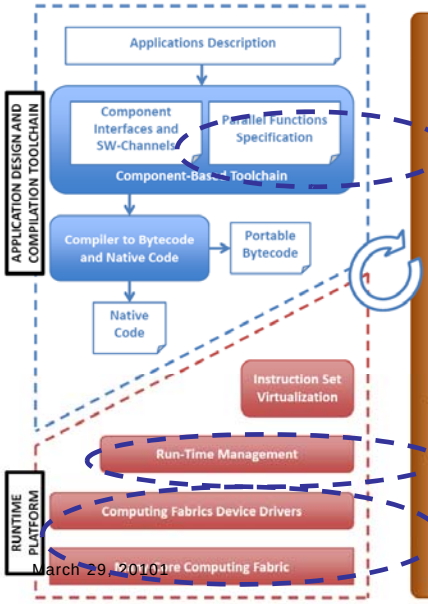
Nucleus Project within UMIC research cluster at RWTH Aachen University

WP3: Co-exploration of Architectural Platforms and Programming Models

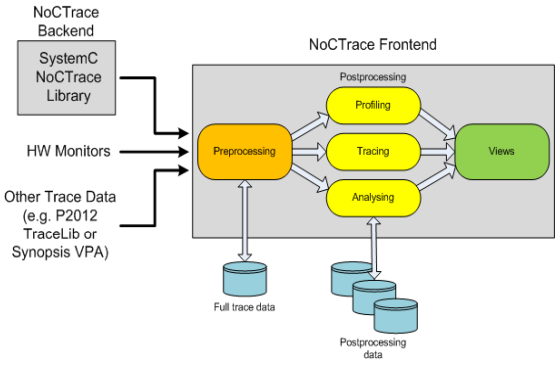


Partners role

- **SYNOPSYS:** EDA tools and virtual platform provider
- **IMEC:** Support for run-time task mapping and scheduling
- **POLIMI:** Design Space Exploration for supporting run-time system management
- **HHI:** Profiling methodology for parallel computing platform. Efficiency analysis of parallel programming models.

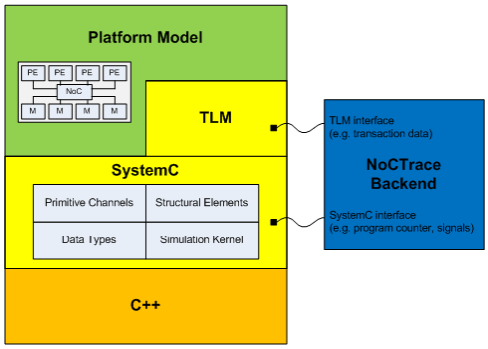
HHI NoCTrace Architecture

- NoCTrace backend
  - collects data
- NoCTrace frontend
  - processes data
  - manages data (persistency)
  - presents data (GUI)

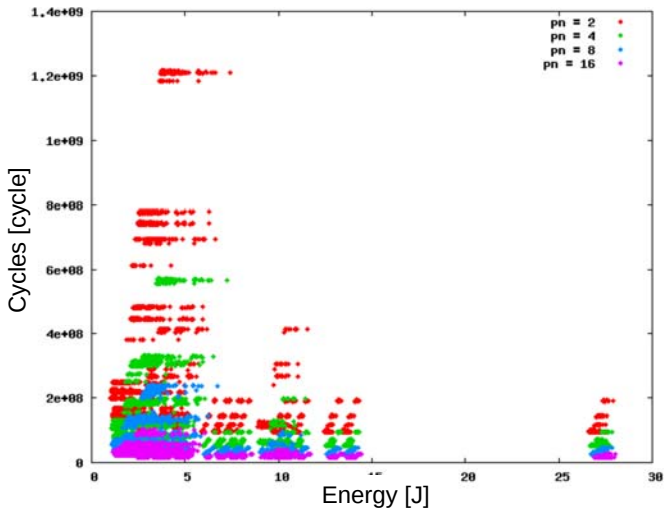


HHI NoCTrace Backend

- Extract/record program counter and transaction data in SystemC kernel
- Perform automatic design analysis to get to know where to place the probes

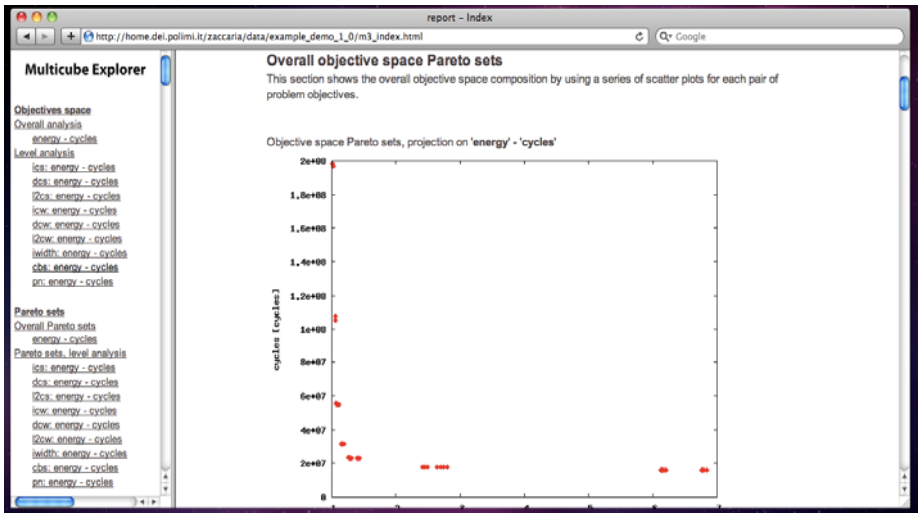


Automatic Multi-Objective Design Space Exploration



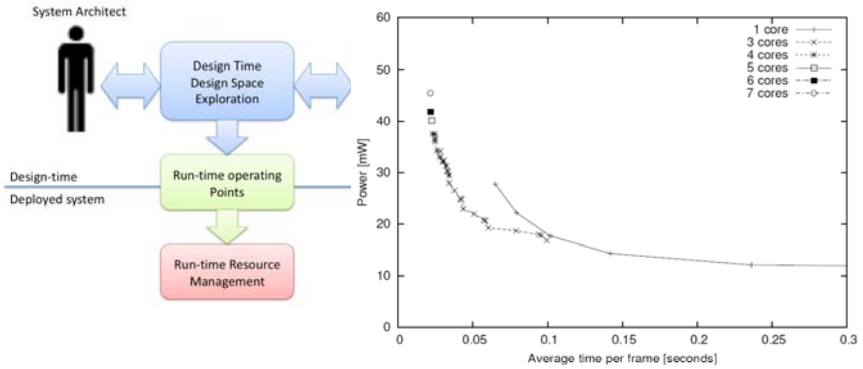
Source: Politecnico di Milano - MPEG2 decoder – MIPS-based multiprocessor – 70nm tech. node – 10 frames

Automatic Multi-Objective Design Space Exploration



Source: Politecnico di Milano - MPEG2 decoder, generated with Multicube Explorer

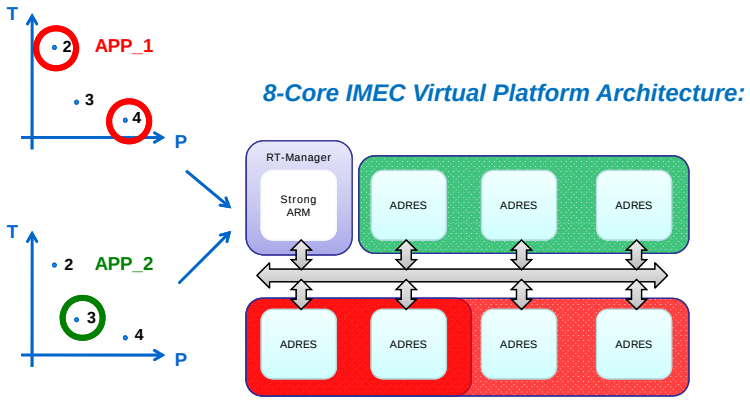
Design-time Exploration to support Run-time Resource Management



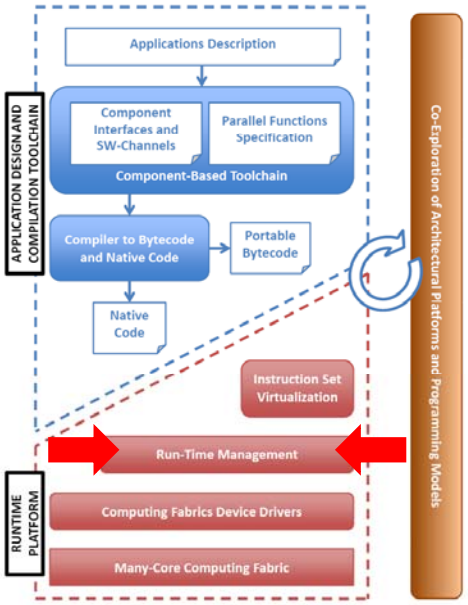
- Based on the **design-time exploration,** we derive a set of Pareto **operating points** corresponding to power, resources (number of cores) and QoS (average time per frame).
- The operating points will be used by the **Run-time Resource Manager** to achieve QoS requirements (average time per frame) while meeting overall resources (number of cores) and minimizing power consumption

Run Time Management of multi-core platform

- The system state can change due to some events:
  - A new application executed or
  - QoS requirements modified



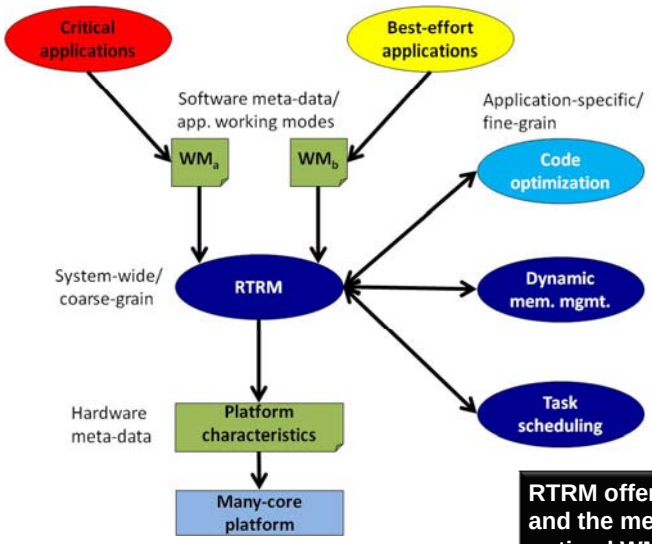
WP4: Runtime Resource Management



Partners role

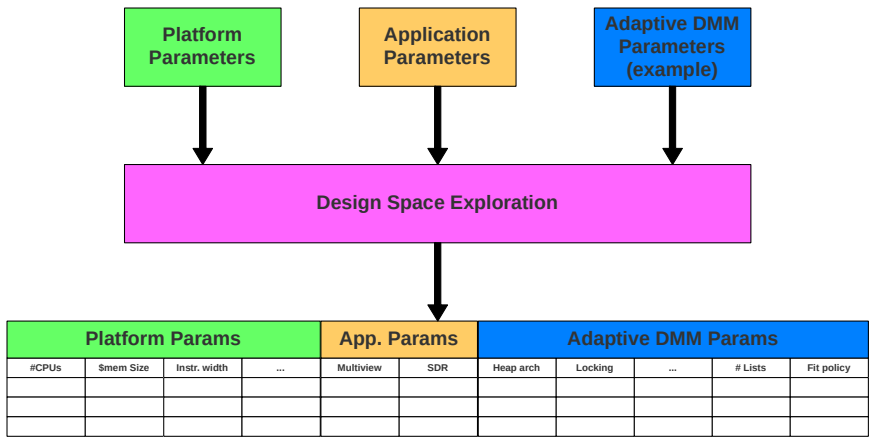
- **ICCS:** Adaptive dynamic data management
- **IMEC:** Adaptive run-time task mapping and scheduling
- **POLIMI:** Run-time QoS constrained resource and power manager at the OS-level
- **STM**: Operating System Integration. Develop-ment of Device Drivers

Run-time resource management (RTRM): Overview



RTRM offers an integrated solution and the mechanisms to perform optimal WM selection at run-time

What is a working mode?



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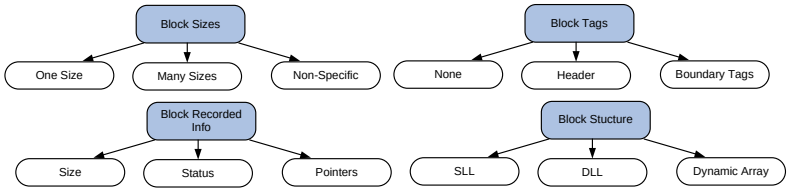
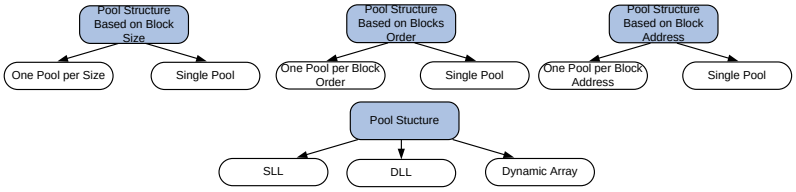
Example of Intra-Heap MTh-DMM Design Space

Intra-Thread Level Design Space

E. Block Structure Decisions



F. Pool Organization Decisions



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